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Question Paper Code : 81280

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Third Semester

Electrical and Electronics Engineering

EE 3302 – DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State De-Morgan's Theorem.
2. List out the different types of output configuration in TTL.
3. Write the significance of K-maps.
4. Mention the applications of multiplexers.
5. Classify synchronous sequential circuits.
6. Name the applications of shift registers.
7. Define critical and non-critical race.
8. Differentiate PLA and PAL.
9. Mention the need for VHDL.
10. Write the data types supported by VHDL.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalents. (6)
- (ii) Explain the Hamming code with an example. State its advantages over parity codes. (7)
- Or
- (b) Explain the characteristics and implementation of the given digital logic families:
- (i) DTL and (6)
- (ii) RTL (7)

12. (a) Design a 3*8 decoder and explain its operation as a minterm generator.

Or

- (b) Write a simplified maxterm Boolean expression for $\Pi(0, 4, 5, 6, 7, 10, 14)$ using the Karnaugh mapping method.

13. (a) (i) Describe the difference between a gated S-R latch and an edge-triggered S-R flip flop. (7)
(ii) Compare the specific features of synchronous and asynchronous counters. (6)

Or

- (b) (i) Design an asynchronous Modulo-8 Down counter using JK flip-flops. (7)
(ii) Differentiate the properties of Mealy and Moore models. (6)

14. (a) Implement the functions $F1(X, Y, Z) = \sum(1, 2, 4, 5)$, $F3(X, Y, Z) = \sum(0, 1, 3, 4)$ and $F2(X, Y, Z) = \sum(2, 3, 6, 7)$ using a single PROM grid.

Or

- (b) Explain the structure of CPLD with the help of block diagram.

15. (a) Write the VHDL code for four-bit adder circuit.

Or

- (b) Write a VHDL Program for 1 to 4 DMUX using data flow modeling.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Simplify the Boolean function using K-map and implement using only NAND gates. $F(A, B, C, D) = \sum m(0, 8, 11, 12, 15) + \sum d(1, 2, 4, 7, 10, 14)$. Mark the essential and non essential prime implicants. (7)
(ii) Explain briefly about SOP and POS forms with an examples. (8)

Or

- (b) (i) Design a half subtractor circuit with inputs x and y and outputs D and B . The circuit subtracts the bits $x-y$ and places the difference in D and the borrow in B . (7)
(ii) Explain the design procedure of RTL using VHDL. (8)